

CHARACTERISTICS OF TRANSISTOR TRANSISTOR LOGIC (TTL)

Aim: To obtain the characteristics of a discrete TTL gate and an Integrated Circuit TTL gate.

Part I. Discrete TTL Gate

A. Experiment

1. Connect the TTL inverter circuit as shown in Fig. 1 using transistors from the CA3046N transistor array. Pin 13 (substrate) has to be always connected ground. Use Q_5 of array for Q_3 in the circuit.
2. Use the X-Y mode of the oscilloscope to observe the transfer characteristics. Apply a 0 to 5V 100Hz triangular wave (adjust dc offset in WAVETEK) to both the input of the logic gate and the X input of the scope. Set the same scale for both X and Y axes and observe the transfer characteristic.
3. By applying 0V and 5V to the input, measure the values of all signal levels. Obtain the values of V_{OH} , V_{OL} , V_{IH} , and V_{IL} . Also calculate their noise margins NM_H and NM_L . Also measure the power dissipated by the gate when the output is high ($P_d(1)$), and the power dissipated when the output is low ($P_d(0)$).
4. Apply a 5V, 200kHz square wave at the input of the TTL gate. Display the input and the output on Channels 1 and 2 respectively with Channel 1 triggered. Measure the rise and fall times of the input waveform. Also measure the propagation delays t_{pHL} and t_{pLH} . Use an external capacitor (1500pF) as load.

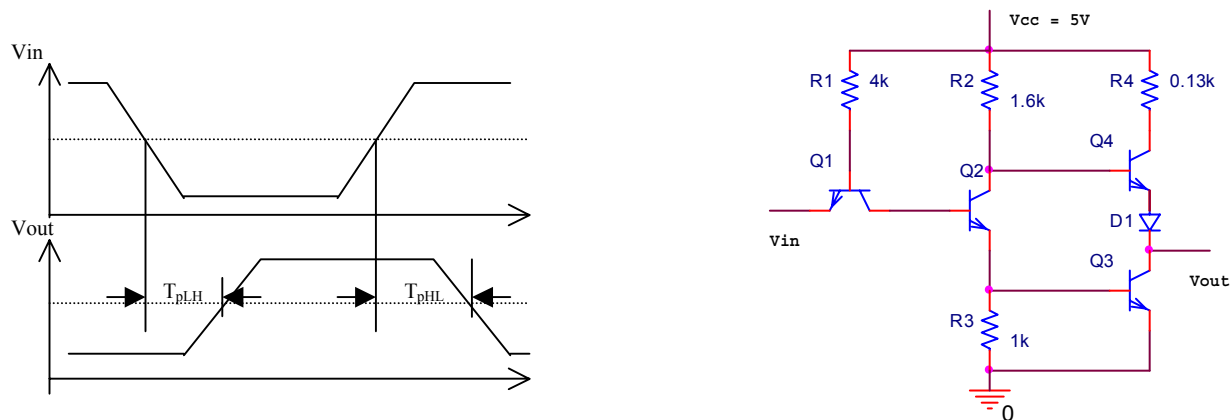


Fig. 1 TTL gate with active pull-up

B. Report

1. Sketch the transfer characteristics observed under A.2.
2. Compare the experimentally measured values under A.3 with the analytically calculated ones.
3. Calculate the net propagation delay $t_p = (t_{pHL} + t_{pLH})/2$.

Part II. TTL Gate with Active Pull-down

Repeat Part I for the TTL gate shown in Fig. 2. Use an external BJT for Q₅. Also under Report Section, compare the transfer characteristics of the gates of Figs 1 and 2 with particular reference to noise margins.

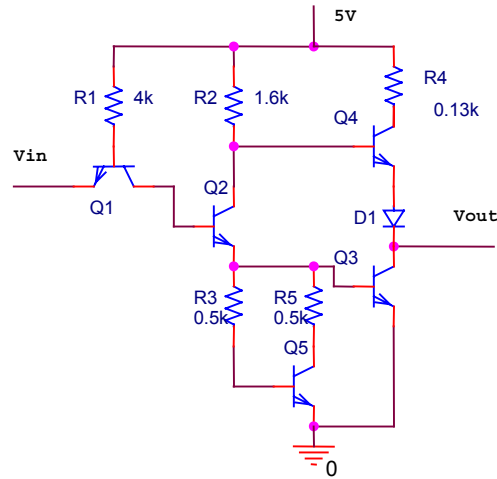


Fig.2 TTL gate with active pull-up and pull-down

Part III. Integrated Circuit TTL Gate

A. Experiment

1. Power the 7404 Hex inverter.
The pin-out diagram is shown in Fig. 3.

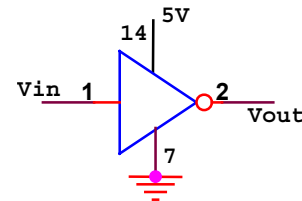


Fig. 3 IC Inverter

2. Obtain the transfer characteristic and transient response of the gate following the steps outlined in Part I of the experiment.
3. Power up the two-input NAND gate 7400 and verify its logic function for a positive logic.

B. Report

1. Obtain the values of V_{OH} , V_{OL} , V_{IH} , and V_{IL} for the 7404 gate. Also calculate their noise margins NM_H and NM_L .